REMARKS

The foregoing amendments are made to correct minor translational errors and to meet United States requirements as to form. No new matter is added.

Respectfully submitted,

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PATENT
Attorney Docket No. 401308

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKAHIRO OHNAKADO

Application No.:	Unassigned	Art Unit:	Unassigned
Filed:	July 25, 2001	Examiner:	Unassigned
For:	SI-MOS HIGH-FREQUENCY SEMICONDUCTOR DEVICE AND THE MANUFACTURING METHOD OF THE SAME		

SPECIFICATION, CLAIMS AND ABSTRACT AS PRELIMINARILY AMENDED

Amendments to the paragraph beginning on page 1, line 2:

The present invention relates to a high-frequency semiconductor device employing an Si-MOS transistor, and especially relates to achievement of a reliable and sophisticated high-frequency semiconductor device having high ESD (Electro Static Discharge) resistance.

Amendments to the paragraph beginning on page 1, line 9:

Mobile phone and wireless LAN ~~are~~ have become widespread in application in recent years, so high-frequency semiconductor ~~device~~ devices, which ~~is~~ are necessary in electric devices ~~of~~ for these uses to improve their performance, have size and ~~costs, has been spotlighted~~ cost concerns. To ~~achieve above~~ produce a high-frequency semiconductor device, a III-V ~~group~~ compound semiconductor, such as GaAs, with high electron mobility is mainly used. However, with ~~minimizing~~ the miniaturization of Si-MOS ~~transistor~~ transistors rapidly in recent years, it ~~becomes~~ has become possible to

form MOS (Metal-Oxide-Semiconductor)~~-transistor of the~~ transistors having a gate length 0.2 μm or less,~~-thereby~~ whereby the transconductance, Gm, of an MOS transistor is greatly improved so that high-frequency characteristics~~-thereof is~~ are improved and ~~becomes~~ the transistors become applicable to high-frequency~~-device for~~ devices in the GHz band. The invention achieves a reliable and sophisticated high-frequency semiconductor device having high ESD (Electro Static Discharge) resistance~~-with~~ employing an MOS transistor of Si.

Amendments to the paragraph beginning on page 2, line 13:

As mentioned above, in the case of ESD, impressing large current into the semiconductor element in a short time~~-result~~ results in melt-down of the element due to ~~heat caused by joule loss~~ heating (this is referred as thermal destruction). Moreover, in case a high voltage caused by ESD is applied to a gate~~-insulting~~ insulating layer of an MOS transistor, which is typically and widely used in recent Si-LSI (Large-Scaled Integration)~~-device~~ devices, breakdown of the gate~~-insulting~~ insulating layer may be caused. Accordingly, these kinds of device destruction caused by ESD, i.e. thermal destruction and breakdown of insulation, are problematic.

Amendments to the paragraph beginning on page 8, line 25:

FIG. 2 is~~-the~~ a circuit diagram illustrating an ESD protection circuit employing an MOS transistor in an OFF state;

Amendments to the paragraph beginning on page 9, line 7:

~~FIG. 6 is a~~FIGs. 6(a)-6(c) are circuit~~-diagram~~ diagrams showing~~-the~~ an ESD protection circuit according to the present invention;

Amendments to the paragraph beginning on page 9, line 11:

FIG. 8 ~~is a figure showing~~ shows a voltage-current characteristic of ~~the~~ a lateral polysilicon ~~diodes~~ diode;

Amendments to the paragraph beginning on page 9, line 13:

FIG. 9 ~~is a figure showing the~~ shows an equivalent circuit for describing outflow of ~~the~~ a high-frequency signal through the parasitic capacitance ~~for~~ of an Si substrate and through the depletion layer ~~capacity~~ capacitance;

Amendments to the paragraph beginning on page 9, line 18:

~~FIG. 11 is a figure showing~~FIGs. 11(a)-11(c) show the influence of the presence of traps ~~of~~ at deep energy levels in ~~the tunnel effect~~ tunneling between bands;

Amendments to the paragraph beginning on page 9, line 20:

~~FIG. 12 is a figure showing~~FIGs. 12(a)-12(c) show the manufacturing process of the high-frequency semiconductor device according to the present invention;

Amendments to the paragraph beginning on page 9, line 23:

~~FIG. 13 is a figure showing~~FIGs. 13(a)-13(c) show the manufacturing process following ~~the~~ FIG. 12(c);

Amendments to the paragraph beginning on page 9, line 25:

~~FIG. 14 is a figure showing~~FIGs. 14(a)-14(c) show the manufacturing process following ~~the~~ FIG. 13(c);

Amendments to the paragraph beginning on page 9, line 27:

~~FIG. 15 is a figure showing~~FIGs. 15(a)-15(c) show the manufacturing following ~~the~~ FIG. 14(c);

Amendments to the paragraph beginning on page 10, line 2:

~~FIG. 16 is a figure showing~~FIGs. 16(a) and 16(b) show the manufacturing process following ~~the~~ FIG. 15(c);

Amendments to the paragraph beginning on page 10, line 5:

~~FIG. 17 is a figure showing~~FIGs. 17(a) and 17(b) show the manufacturing process following ~~the~~ FIG. 16(b);

Amendments to the paragraph beginning on page 10, line 6:

~~FIG. 18 is a figure showing~~FIGs. 18(a)-18(c) show other manufacturing ~~process~~ processes of the high-frequency semiconductor device according to the present invention;

Amendments to the paragraph beginning on page 10, line 9:

~~FIG. 19 is a figure showing~~FIGs. 19(a)-19(c) show the manufacturing process following ~~the~~ FIG. 18(c);

Amendments to the paragraph beginning on page 10, line 11:

~~FIG. 20 is a figure showing~~FIGs. 20(a)-20(c) show the manufacturing process following ~~the~~ FIG. 19(c);

Amendments to the paragraph beginning on page 10, line 13:

~~FIG. 21 is a figure showing further~~FIGs. 21(a)-21(c) show still other manufacturing ~~process~~ processes of the high-frequency semiconductor device according to the present invention;

Amendments to the paragraph beginning on page 10, line 16:

~~FIG. 22 is a figure showing~~FIGs. 22(a)-22(c) show the manufacturing process following ~~the~~ FIG. 21(c);

Amendments to the paragraph beginning on page 10, line 18:

~~FIG. 23 is a figure showing~~FIGs. 23(a) and 23(b) show the manufacturing process following ~~the~~ FIG. 22(c);

Amendments to the paragraph beginning on page 10, line 20:

~~FIG. 24 is a figure showing~~FIGs. 24(a) and 24(b) show the manufacturing process following ~~the~~ FIG. 23(b);

Amendments to the paragraph beginning on page 10, line 22:

~~FIG. 25 is a figure showing further~~FIGs. 25(a)-25(c) show still other manufacturing ~~process~~ processes of the high-frequency semiconductor device according to the present invention;

Amendments to the paragraph beginning on page 10, line 25:

~~FIG. 26 is a figure showing~~FIGs. 26(a)-26(c) show the manufacturing process following ~~the~~ FIG. 25(c);

Amendments to the paragraph beginning on page 10, line 27:

~~FIG. 27 is a figure showing~~FIGs. 27(a) and 27(b) show the manufacturing process following ~~the~~ FIG. 26(c);

Amendments to the paragraph beginning on page 11, line 2:

~~FIG. 28 is a figure showing~~FIGs. 28(a) and 28(b) show the manufacturing process following ~~with the~~ FIG. 27(b);

Amendments to the paragraph beginning on page 11, line 4:

~~FIG. 29 is a figure showing~~FIGs. 29(a) and 29(b) show an example of a PN junction of a lateral polysilicon ~~diodes~~ diode;

Amendments to the paragraph beginning on page 11, line 6:

~~FIG. 30 is a figure showing other~~FIGs. 30(a) and 30(b) show another example of a PN junction of a lateral polysilicon ~~diodes~~ diode;

Amendments to the paragraph beginning on page 11, line 8:

~~FIG. 31 is a figure showing~~FIGs. 31(a) and 31(b) show still ~~other~~ another example of a PN junction of a lateral polysilicon ~~diodes~~ diode;

Amendments to the paragraph beginning on page 11, line 11:

~~FIG. 32 is a figure showing further~~FIGs. 32(a) and 32(b) show still ~~other~~ another example of a PN junction of a lateral polysilicon ~~diodes~~ diode;

Amendments to the paragraph beginning on page 11, line 14:

~~FIG. 34 is a figure showing~~FIGs. 34(a)-34(c) show a clamp circuit connected between VDD and GND according to the present invention;

Amendments to the paragraph beginning on page 11, line 18:

FIG. 36~~ is a figure showing other~~ shows another example of a clamp circuit connected between VDD and GND.

Amendments to the paragraph beginning on page 11, line 24:

~~FIG. 6 shows~~FIGs. 6(a)-6(c) show an arrangement of an ESD protection circuit for ~~the~~ a high-frequency semiconductor device according to the present invention. ~~FIG. 7 shows~~FIGs. 7(a) and 7(b) show the structure of an ESD protection element. In the ESD protection circuit according to the present embodiment, the lateral polysilicon diodes, which are formed with polysilicon (~~polycrystal~~polycrystalline silicon ~~layer~~) for forming gate electrodes of the Si-MOS transistor, are employed. By the lateral polysilicon diodes, the clamp circuit for ESD is composed.

Amendments to the paragraph beginning on page 21, line 26:

The manufacturing process of the high-frequency semiconductor device of ~~embodiment~~ embodiments 1, 2, and 3 are described ~~with~~ referring to ~~FIG. 12, 13, 14, 15, 16, and 17~~ FIGs. 12(a)-17(b). ~~FIG. 12, 13, 14, 15, 16, and 17 shows~~FIGs. 12(a)-17(c) show a manufacturing process of high-frequency semiconductor device in which an NMOS transistor, a PMOS transistor, and lateral polysilicon diodes are formed on region 91 for NMOS, region 92 for PMOS, and region 93 for ~~diode~~ diodes, respectively.

Amendments to the paragraph beginning on page 24, line 11:

Another example of the manufacturing process of the high-frequency semiconductor device of embodiments 1, 2, and 3 ~~are~~ is described ~~with~~ referring to ~~FIG. 18, 19, and 20~~ FIGs. 18(a)-20(c). ~~FIG. 18, 19, and 20 shows~~FIGs. 18(a)-20(c) show the manufacturing process of the high-frequency semiconductor device wherein an NMOS transistor, a PMOS transistor, and the lateral polysilicon diodes are formed on the region 91 for NMOS, region 92 for PMOS, and region 93 for ~~diode~~ diodes, respectively.

Amendments to the paragraph beginning on page 26, line 5:

Another manufacturing process of the high-frequency semiconductor device of ~~embodiment~~ embodiments 1, 2, and 3 ~~are~~ is described ~~with~~ referring to ~~FIG. 21,22,23 and 24~~ FIGS. 21(a)-24(b). ~~FIG.21, 22, 23 and 24~~FIGs. 21(a)-24(b) show the manufacturing process of the high-frequency semiconductor device wherein an NMOS transistor, a PMOS transistor, ~~a~~ lateral polysilicon diodes, and a capacitor are formed on the region 91 for NMOS, region 92 for PMOS, region 93 for ~~diode~~ diodes, and region 94 for a capacitor, respectively.

Amendments to the paragraph beginning on page 28, line 5:

Another manufacturing process of the high-frequency semiconductor device of ~~embodiment~~ embodiments 1, 2, and 3 ~~are~~ is described ~~with~~ referring to ~~FIG. 25, 26, 27 and 28~~ FIGs. 25(a)-28(b). ~~FIG.25, 26, 27 and 28~~FIGs. 25(a)-28(b) show the manufacturing process of the high-frequency semiconductor device wherein an NMOS transistor, a PMOS transistor, ~~a~~ lateral polysilicon diodes, and a insulating film of the capacitor are formed on the region 91 for NMOS, region 92 for PMOS, region 93 for ~~diode~~ diodes, and region 94 for a capacitor, respectively.

Amendments to the paragraph beginning on page 30, line 10:

The method of forming lateral polysilicon diodes ~~in above-mentioned embodiment~~ of embodiments 4, 5, 6, and 7 will be further described in detail ~~with~~ referring to ~~FIG. 29, 30, 31, and 32~~ FIGs. 29(a)-32(b).

Amendments to the paragraph beginning on page 34, line 22:

Therefore, in the present embodiment, as shown in FIG.34(a), a clamp circuit 48, which starts operating at a lower voltage than the reverse breakdown voltage of the lateral polysilicon diode, is ~~attached~~ connected between the external power supply VDD and the ground GND.

Amendments to the existing claims:

1. (Amended) A high-frequency semiconductor device comprising:

a substrate; and

~~a~~ an Si MOS transistor and a first lateral polysilicon diode ~~both formed~~ on ~~a~~ the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line ~~and~~ to an externally supplied voltage VDD~~, and forward direction of the lateral polysilicon diode is direction from the high-frequency I/O signal line to the externally supplied voltage VDD~~.

2. (Amended) ~~A~~The high-frequency semiconductor device of Claim 1, further comprising a second lateral polysilicon diode on the substrate and having a forward direction and a reverse direction, wherein the second lateral polysilicon diode connects, in the forward direction, ground, GND ~~and a~~, to the high-frequency I/O signal line~~, and forward direction of the lateral polysilicon diode is direction from ground GND to the high-frequency I/O signal line~~.

3. (Amended) ~~A~~The high-frequency semiconductor device of Claim 2,~~wherein~~ including m lateral polysilicon diodes~~to the number of "m" are~~ connected in series between the high-frequency I/O signal line and the externally supplied voltage, VDD~~in series~~, and n lateral polysilicon diodes~~to the number of "n" are~~ connected in series between the ground, GND, and the high-frequency I/O signal line~~in series, and with assuming the voltage of VDD as V_{dd}, V_{dd}/(n+m)~~ wherein VDD/(n+m) is smaller than 1.1 ~~(V)~~ volts.

4. (Amended) ~~A~~The high-frequency semiconductor device of Claim 1, wherein~~a~~ no lateral polysilicon diode is~~not~~ connected to~~a~~ any signal line other than~~a~~ the high frequency I/O signal line.

5. (Amended) ~~A~~The high-frequency semiconductor device of Claim 1 further comprising a capacitor having~~a~~ lower~~electrode~~ and~~an~~ upper~~electrode both formed with~~ polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor are~~formed~~ from~~same~~ a first polysilicon layer, and~~gate electrode of~~ the MOS transistor~~is formed from another~~ has a polysilicon gate electrode from a second polysilicon layer.

6. (Amended) ~~A~~The high-frequency semiconductor device of Claim 1 further comprising a capacitor having~~a~~ lower~~electrode~~ and~~an~~ upper~~electrode both formed with~~ polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor are~~formed~~ from~~same~~ a first polysilicon layer,~~and gate electrode of~~ the MOS transistor has a polysilicon gate, and the upper electrode of the capacitor~~are formed from another~~ and the gate are from a second polysilicon layer.

7. (Amended) ~~A~~The high-frequency semiconductor device of claim 5, wherein the polysilicon layer~~to form~~ of the upper electrode of the capacitor~~is also left on and covering~~ covers a PN junction of the first lateral polysilicon diode.

8. (Amended) ~~A~~The high-frequency semiconductor device of claim 5, wherein the capacitor includes a dielectric layer ~~to form the capacitor is also left on~~ and ~~covering~~ the dielectric layer covers a PN junction of the first lateral polysilicon diode.

9. (Amended) A ~~manufacturing~~ method of manufacturing a high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes, and a capacitor on a substrate, and a first of the lateral polysilicon ~~diode connects~~ diodes connects a high-frequency I/O signal line ~~and~~ to an externally supplied voltage, VDD, and ~~the other~~ a second of lateral polysilicon ~~diode connects~~ diodes connects ground, GND ~~and~~, to the high-frequency I/O signal line ~~; wherein~~, the method comprising:

forming a first polysilicon layer and a lower electrode of the capacitor and the lateral polysilicon ~~diode are formed~~ diodes from ~~a~~ the first polysilicon layer ~~, the~~:

forming a first dielectric layer as an insulating film of the capacitor ~~is formed from a first dielectric layer, the~~;

forming a second polysilicon layer and an upper electrode of the capacitor ~~is formed~~ from ~~a~~ the second polysilicon layer, wherein the first dielectric layer ~~is also left on~~ covers a ~~certain~~ region of the first polysilicon layer at which PN ~~junction~~ junctions of the lateral polysilicon ~~diode is~~ diodes are to be formed ~~,~~; and ~~an edge of~~

forming a resist mask ~~used~~, for injecting ~~ion~~ ions into an N-type region of the lateral polysilicon diode and ~~an edge of a resist mask used~~ for injecting ~~ion~~ ions into ~~the~~ a P-type region of the lateral polysilicon diode ~~are placed~~, on the first dielectric layer ~~being left~~.

10. (Amended) A ~~manufacturing~~ method of manufacturing a high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes, and a capacitor on a substrate, and a first of the lateral polysilicon ~~diode connects~~ diodes connects a high-frequency I/O signal line ~~and~~ to an externally supplied voltage, VDD, and ~~the other~~ a second of lateral polysilicon ~~diode connects~~ diodes connects ground, GND ~~and~~, to the high-frequency I/O signal line ~~; wherein~~, the method comprising:

forming a first polysilicon layer and a lower electrode of the capacitor and the lateral polysilicon ~~diode are formed~~ diodes from ~~a~~ the first polysilicon layer ~~, the~~:

forming a first dielectric layer as an insulating film of the capacitor ~~is formed from a first dielectric layer, the~~;

forming a second polysilicon layer and an upper electrode of the capacitor ~~is formed~~ from ~~a~~ the second polysilicon layer, wherein the second polysilicon layer ~~is also left on~~ covers a ~~certain~~ region of the first polysilicon layer at which PN ~~junction~~ junctions of the lateral polysilicon ~~diode is~~ diodes are to be formed~~,~~; and ~~an edge of~~

forming a resist mask ~~used~~, for injecting ~~ion~~ ions into an N-type region of the lateral polysilicon diode and ~~an edge of a resist mask used~~ for injecting ~~ion~~ ions into ~~the~~ a P-type region of the lateral polysilicon diode ~~are placed~~, on the second polysilicon layer ~~being left~~.

11. (Amended) ~~A~~The manufacturing method of claim 9, ~~wherein~~ including forming a gate electrode of the MOS transistor ~~is formed~~ from the second polysilicon layer.

12. (Amended) ~~A~~The high-frequency semiconductor device of claim 1 further comprising a clamp circuit connected between the externally supplied voltage, VDD, and ground, GND, wherein the clamp circuit ~~operates to flow~~ permits current ~~within~~ flow at a voltage lower than ~~the absolute value of~~ a reverse bias breakdown voltage of the first lateral polysilicon diode.

Amendments to the abstract:

Abstract of the Disclosure

~~An object of the present invention is to provide a~~A sophisticated and highly reliable high-frequency Si-MOS semiconductor device having high electrostatic discharge (ESD) resistance. ~~In the semiconductor device according to the present invention, lateral~~Lateral polysilicon diodes are ~~formed and~~ connected between high-frequency I/O signal ~~line~~ lines and the external supply voltage, VDD, and between the ground, GND, and the high-frequency I/O signal ~~line~~ lines, respectively. The forward direction of the diodes is the direction from the high-frequency I/O signal line to the supply voltage,

VDD_s and the direction from the ground, GND_s to the high-frequency I/O signal line, respectively.

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKAHIRO OHNAKADO

Application No.:	Unassigned	Art Unit:	Unassigned
Filed:	July 25, 2001	Examiner:	Unassigned
For:	SI-MOS HIGH-FREQUENCY SEMICONDUCTOR DEVICE AND THE MANUFACTURING METHOD OF THE SAME		

CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A high-frequency semiconductor device comprising:

a substrate; and

an Si MOS transistor and a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage VDD.

2. The high-frequency semiconductor device of Claim 1, further comprising a second lateral polysilicon diode on the substrate and having a forward direction and a reverse direction, wherein the second lateral polysilicon diode connects, in the forward direction, ground, GND, to the high-frequency I/O signal line.

3. The high-frequency semiconductor device of Claim 2, including m lateral polysilicon diodes connected in series between the high-frequency I/O signal line and the externally supplied voltage, VDD, and n lateral polysilicon diodes connected in series

between the ground, GND, and the high-frequency I/O signal line wherein VDD/(n+m) is smaller than 1.1 volts.

4. The high-frequency semiconductor device of Claim 1, wherein no lateral polysilicon diode is connected to any signal line other than the high frequency I/O signal line.

5. The high-frequency semiconductor device of Claim 1 further comprising a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor are from a first polysilicon layer, and the MOS transistor has a polysilicon gate electrode from a second polysilicon layer.

6. The high-frequency semiconductor device of Claim 1 further comprising a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor are from a first polysilicon layer, the MOS transistor has a polysilicon gate, and the upper electrode of the capacitor and the gate are from a second polysilicon layer.

7. The high-frequency semiconductor device of claim 5, wherein the polysilicon layer of the upper electrode of the capacitor covers a PN junction of the first lateral polysilicon diode.

8. The high-frequency semiconductor device of claim 5, wherein the capacitor includes a dielectric layer and the dielectric layer covers a PN junction of the first lateral polysilicon diode.

9. A method of manufacturing a high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes, and a capacitor on a substrate, and a first of the lateral polysilicon diodes connects a high-frequency I/O signal line to an externally

supplied voltage, VDD, and a second of lateral polysilicon diodes connects ground, GND, to the high-frequency I/O signal line, the method comprising:

forming a first polysilicon layer and a lower electrode of the capacitor and the lateral polysilicon diodes from the first polysilicon layer:

forming a first dielectric layer as an insulating film of the capacitor;

forming a second polysilicon layer and an upper electrode of the capacitor from the second polysilicon layer, wherein the first dielectric layer covers a region of the first polysilicon layer at which PN junctions of the lateral polysilicon diodes are to be formed; and

forming a resist mask, for injecting ions into an N-type region of the lateral polysilicon diode and for injecting ions into a P-type region of the lateral polysilicon diode, on the first dielectric layer.

10. A method of manufacturing a high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes, and a capacitor on a substrate, and a first of the lateral polysilicon diodes connects a high-frequency I/O signal line to an externally supplied voltage, VDD, and a second of lateral polysilicon diodes connects ground, GND, to the high-frequency I/O signal line, the method comprising:

forming a first polysilicon layer and a lower electrode of the capacitor and the lateral polysilicon diodes from the first polysilicon layer:

forming a first dielectric layer as an insulating film of the capacitor;

forming a second polysilicon layer and an upper electrode of the capacitor from the second polysilicon layer, wherein the second polysilicon layer covers a region of the first polysilicon layer at which PN junctions of the lateral polysilicon diodes are to be formed; and

forming a resist mask, for injecting ions into an N-type region of the lateral polysilicon diode and for injecting ions into a P-type region of the lateral polysilicon diode, on the second polysilicon layer.

11. The manufacturing method of claim 9, including forming a gate electrode of the MOS transistor from the second polysilicon layer.

12. The high-frequency semiconductor device of claim 1 further comprising a clamp circuit connected between the externally supplied voltage, VDD, and ground, GND, wherein the clamp circuit permits current flow at a voltage lower than a reverse bias breakdown voltage of the first lateral polysilicon diode.